This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-22. Cancelled.

The following new claims have been added.

23. (New) A method for filling a via hole in a FSG layer comprising:

depositing the FSG layer on a substrate;

depositing a USG layer on the FSG layer;

patterning and then etching said USG and FSG layers to form a via hole having walls and extending down to th e substrate;

forming a seed layer on the walls of the via hole;

overfilling the via hole with a predetermined material; and

by means of CMP, removing said predetermined material.

24. (New) The method of claim 23 wherein depositing the FSG layer comprises depositing the FSG layer to a thickness between about 0.2 and 1 microns with between about 3 and 10 atomic percent fluorine.

25. (New) The method of claim 23 wherein depositing the USG layer comprises depositing the USG layer to a thickness between about 0.1 and 0.2 microns.

26. (New) The method of claim 23 wherein depositing the USG layer further comprises using PECVD from silane or TEOS at about 400° C.

27. (New) A method for forming a single damascene connector comprising:

depositing on a partially completed integrated circuit a layer of FSG;

depositing a layer of USG on the FSG layer;

on the USG layer, depositing a layer of silicon oxynitride;

patterning and then etching the silicon oxynitride, USG, and FSG layers, thereby forming a via hole extending down to the partially completed integrated circuit;

depositing a barrier layer on all walls of the via hole;

depositing a copper seed layer on the barrier layer;

overfilling the via hole with copper; and

by means of CMP, removing the copper until the USG layer is reached, thereby forming the damascene connector.

28. (New) The method of claim 27 wherein depositing the USG layer further comprises using PECVD from silane or TEOS at about 400° C.

29. (New) The method of claim 27 wherein depositing the USG layer comprises depositing the USG layer to a thickness between about 0.1 and 0.2 microns.

30. (New) The method of claim 27 wherein removing the copper until the USG layer is reached further comprises detecting the USG layer by detecting a change in reflectivity.

31. (New) A method for forming a dual damascene connector comprising:

depositing a layer of silicon nitride on a partially completed integrated circuit;

on said layer of silicon nitride, depositing a layer of FSG;

depositing a layer of USG on the FSG layer;

on the USG layer, depositing a layer of silicon oxynitride for use as an anti-reflection coating;

patterning and then etching the silicon oxynitride, USG, and FSG layers, thereby forming a trench;

patterning and then etching the FSG layer, including the trench, whereby a via hole extending as far as the layer of silicon nitride is formed inside the trench;

selectively removing the layer of silicon nitride;

depositing a barrier layer on all walls of the trench and the via hole;

depositing a copper seed layer on the barrier layer;

overfilling the via hole and the trench with copper; and

by means of CMP, removing the copper until the USG layer is reached, thereby forming the damascene connector.

32. (New) The method of claim 31 wherein deposing the layer of silicon nitride comprises depositing the silicon nitride to a thickness between about 300 and 1,000 Angstroms.

33. (New) The method of claim 31 wherein depositing the layer of silicon oxynitride comprises depositing the silicon oxynitride to a thickness between about 400 and 1,500 Angstroms.

34. (New) The method of claim 31 wherein removing the copper until said USG layer is reached further comprises optically detecting of the USG layer through a change in reflectivity.

35. (New) A semiconductor device comprising:

a layer of FSG disposed on a substrate;

a layer of USG, having an upper surface, disposed on the layer of FSG;

a via hole extending from the upper surface to the substrate; and

the via hole being filled with a predetermined material.

36. (New) The semiconductor device of claim 35 wherein the FSG layer is between about 0.4 and 1 microns thick and contains between about 3 and 10 atomic percent fluorine.

37. (New) The semiconductor device of claim 35 wherein the USG layer is between about 0.1 and 0.2 microns thick.

38. (New) A single damascene connector, comprising:

a layer of FSG on a partially completed integrated circuit;

a layer of USG, having a first upper surface, on the layer of FSG;

a via hole extending from the first upper surface down to the integrated circuit;

a barrier layer on all walls of the via hole; and

the via hole being filled with copper having a second upper surface that is substantially flush with the first upper surface.

39. (New) The single damascene connector of claim 38 wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, titanium nitride, and titanium silicon nitride.

40. (New) The single damascene connector of claim 38 wherein the barrier layer is between about 50 and 500 Angstroms thick.

41. (New) A dual damascene connector, comprising:

a layer of FSG on a partially completed integrated circuit;

a layer of USG, having a first upper surface, on the layer of FSG;

a trench, extending from the first upper surface through the USG layer a distance into the FSG layer, the trench having first sidewalls and a floor;

a via hole, having second sidewalls, extending from the trench floor through the FSG layer down to the integrated circuit;

a barrier layer on the first and second sidewalls and on the trench floor; and

the via hole and trench being filled with copper and having a second upper surface substantially flush with the first upper surface.

42. (New) The dual damascene connector of claim 41 wherein the trench has a width between about 0.1 and 1 microns and a depth between about 0.2 and 1 microns.

43. (New) The dual damascene connector of claim 41 wherein the via hole has a width between about 0.1 and 0.6 microns and a depth between about 0.4 and 1 microns.

44. (New) The dual damascene connector of claim 41 wherein the USG layer is between about 0.1 and 0.2 microns thick.